

54AC/74AC74 • 54ACT/74ACT74 Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q , $\bar{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

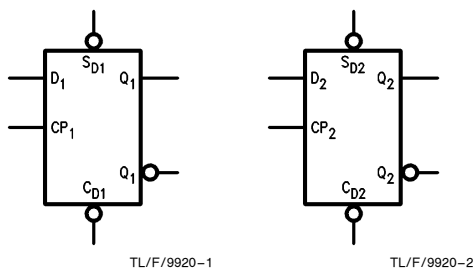
Asynchronous Inputs:

LOW input to $\bar{S}_D$ (Set) sets Q to HIGH level
LOW input to $\bar{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$ makes both Q and $\bar{Q}$ HIGH

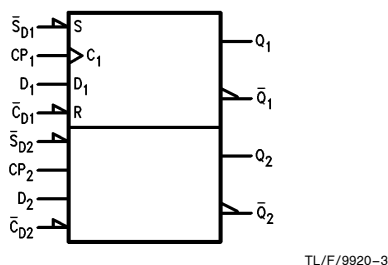
Features

- I_{CC} reduced by 50%
- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'AC74: 5962-88520
 - 'ACT74: 5962-87525

Logic Symbols



IEEE/IEC

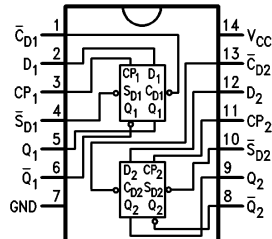


TL/F/9920-3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs
$Q_1, \bar{Q}_1, Q_2, \bar{Q}_2$	Outputs

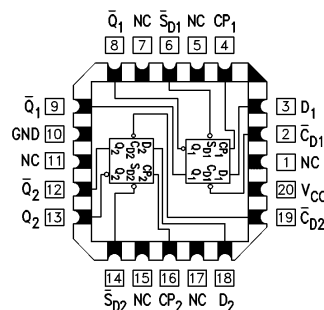
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9920-4

Pin Assignment for LCC



TL/F/9920-5

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Truth Table (Each Half)

Inputs				Outputs	
$\bar{S}_D$	$\bar{C}_D$	CP	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = HIGH Voltage Level

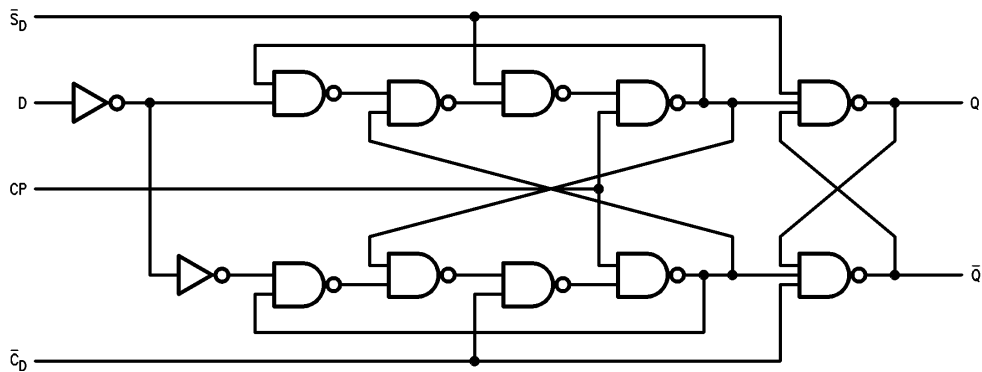
L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

$Q_0(\bar{Q}_0)$ = Previous Q($\bar{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.5	0.44		
		5.5		0.36	0.5	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74AC		54AC	74AC	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		2.0	40.0	20.0	μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		54ACT	74ACT	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = −24 mA
		5.5		4.86	4.70	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA
		5.5		0.36	0.50	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5	mA	V _I = V _{CC} − 2.1V
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		2.0	40.0	20.0	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74AC			54AC		74AC		Units
			T _A = + 25°C C _L = 50 pF			T _A = − 55°C to + 125°C C _L = 50 pF		T _A = − 40°C to + 85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		70 95		95 125		MHz
t _{PLH}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	3.3 5.0	3.5 2.5	8.0 6.0	12.0 9.0	1.0 1.0	13.0 9.5	2.5 2.0	13.0 10.0	ns
t _{PHL}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	3.3 5.0	4.0 3.0	10.5 8.0	12.0 9.5	1.0 1.0	14.0 10.5	3.5 2.5	13.5 10.5	ns
t _{PLH}	Propagation Delay CP _n to Q _n or Q̄ _n	3.3 5.0	4.5 3.5	8.0 6.0	13.5 10.0	1.0 1.0	17.5 12.0	4.0 3.0	16.0 10.5	ns
t _{PHL}	Propagation Delay CP _n to Q _n or Q̄ _n	3.3 5.0	3.5 2.5	8.0 6.0	14.0 10.0	1.0 1.0	13.5 10.0	3.5 2.5	14.5 10.5	ns

*Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74AC		54AC	74AC	Units
			T _A = +25°C C _L = 50 pF		T _A = −55°C to +125°C C _L = 50 pF	T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum			
t _s	Set-up Time, HIGH or LOW D _n to CP _n	3.3 5.0	1.5 1.0	4.0 3.0	5.0 4.0	4.5 3.0	ns
t _h	Hold Time, HIGH or LOW D _n to CP _n	3.3 5.0	−2.0 −1.5	0.5 0.5	0.5 0.5	0.5 0.5	ns
t _w	CP _n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	8.0 5.5	7.0 5.0	ns
t _{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −2.0	0 0	0.5 0.5	0 0	ns

*Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units
			T _A = + 25°C C _L = 50 pF			T _A = − 55°C to + 125°C C _L = 50 pF		T _A = − 40°C to + 85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{max}	Maximum Clock Frequency	5.0	145	210		85		125		MHz
t _{PLH}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	5.0	3.0	5.5	9.5	1.0	11.5	2.5	10.5	ns
t _{PHL}	Propagation Delay C̄ _{Dn} or S̄ _{Dn} to Q _n or Q̄ _n	5.0	3.0	6.0	10.0	1.0	12.5	3.0	11.5	ns
t _{PLH}	Propagation Delay CP _n to Q _n or Q̄ _n	5.0	4.0	7.5	11.0	1.0	14.0	4.0	13.0	ns
t _{PHL}	Propagation Delay CP _n to Q _n or Q̄ _n	5.0	3.5	6.0	10.0	1.0	12.0	3.0	11.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74ACT		54ACT		74ACT		Units
			T _A = +25°C C _L = 50 pF		T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Typ	Guaranteed Minimum					
t _s	Set-up Time, HIGH or LOW D _n to CP _n	5.0	1.0	3.0	4.0	3.5	ns		
t _h	Hold Time, HIGH or LOW D _n to CP _n	5.0	−0.5	1.0	1.0	1.0	ns		
t _w	CP _n or $\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ Pulse Width	5.0	3.0	5.0	7.0	6.0	ns		
t _{rec}	Recovery Time $\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ to CP	5.0	−2.5	0	0.5	0	ns		

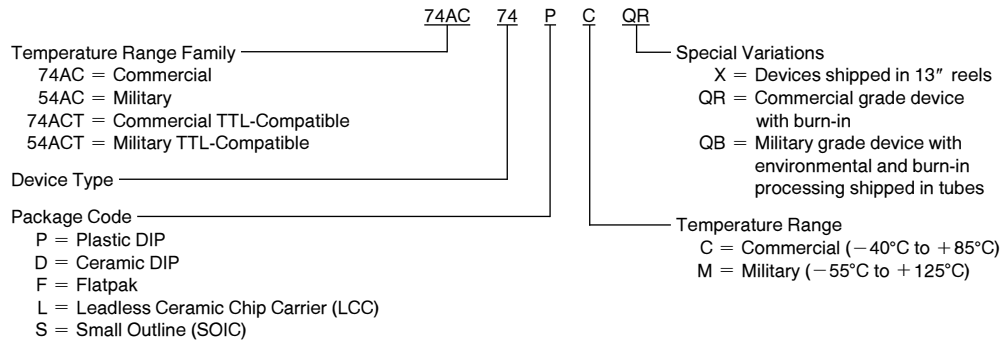
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

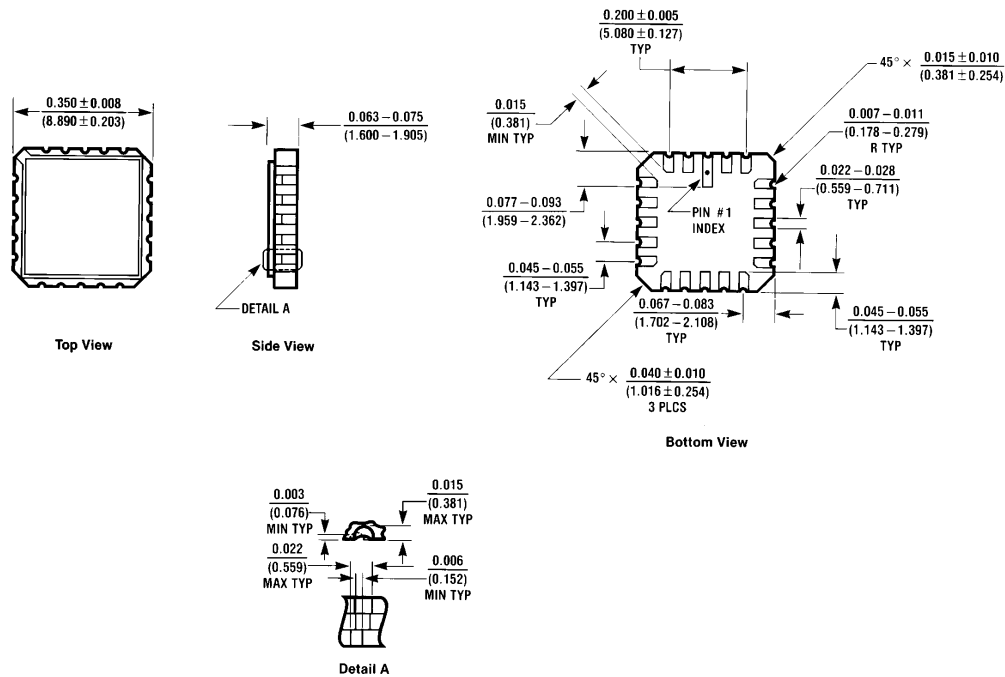
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	35.0	pF	V _{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

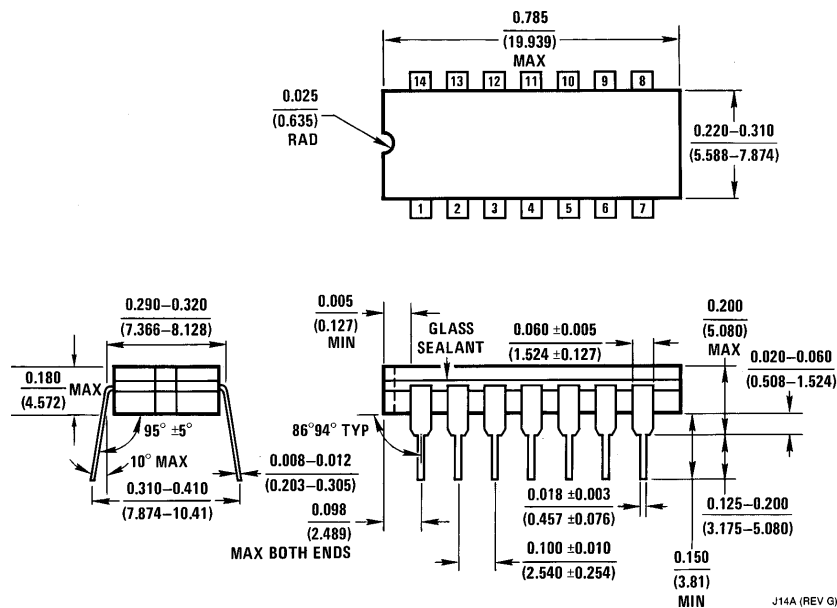


Physical Dimensions inches (millimeters)



**20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

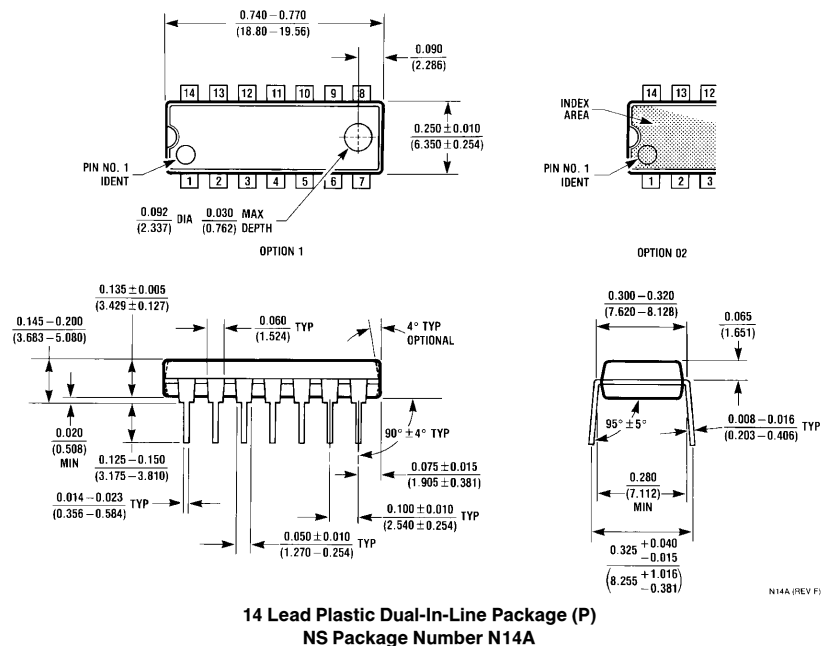
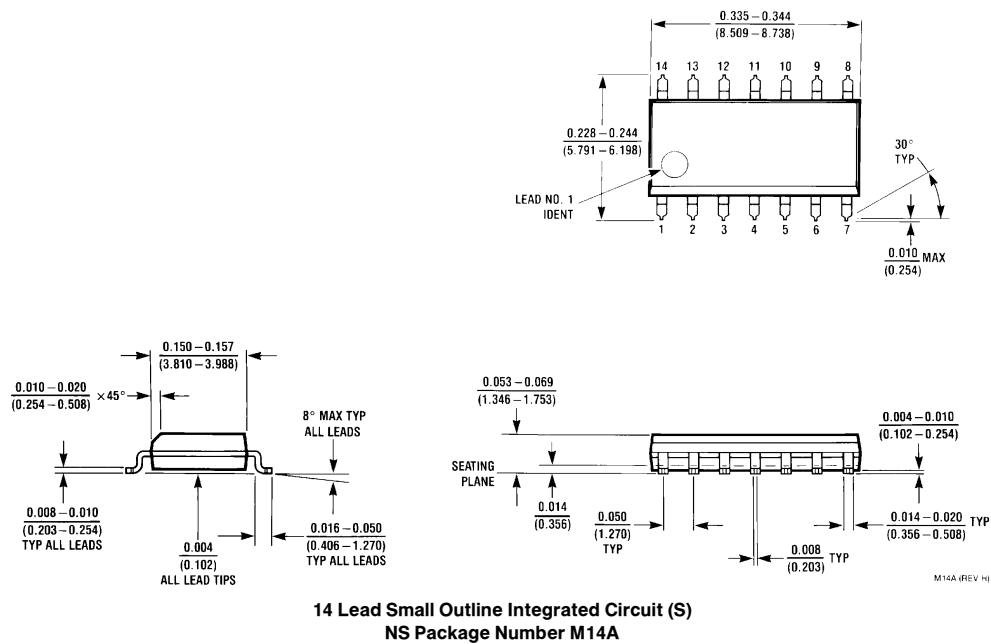
E20A (REV D)

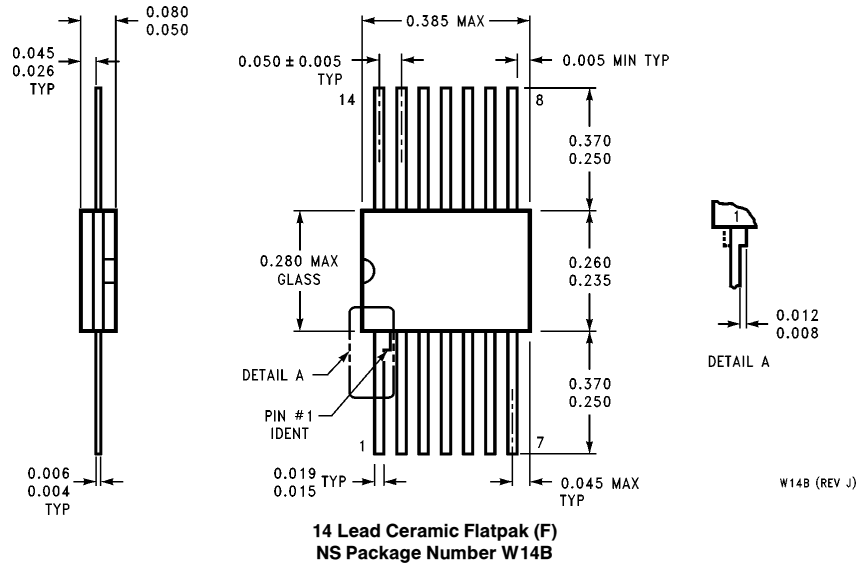


**14 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A**

J14A (REV G)

Physical Dimensions inches (millimeters) (Continued)



Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

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